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10/830,068

04/23/2004

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EXAMINER

GUHARAY, KARABI

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/830,068	Applicant(s) AHN, YOUNG JOON	
	Examiner Karabi Guharay	Art Unit 2889	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Amendment, filed on 3/6/2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,5,7,9,11-13,26-32,34-36 and 39-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,9,11-13,26-32,34-36 and 39-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

Amendment, filed on 3/6/08 has been considered and entered.

Claim 8 is canceled. New claims 43-45 are added.

Currently, claims 1, 3, 5, 7, 9, 11-13, 26-32, 34-36 and 39-45 are pending.

Specification

The disclosure is objected to because of the following informalities: Specification paragraph 0085 recites “by spreading buffer layer material on the upper substrate 316 where the sustain electrode pair 304Y, 304Z have been formed” .However, Figs 12 shows buffer layer is not formed on the upper substrate where the sustain electrode pair 304Y, 304Z have been formed. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7, 9, 26-28, 30-31, 39-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (US 2002/0036466).

Regarding claims 1 & 40, Tanaka et al. disclose a plasma display panel (Fig 2), comprising: a first substrate (11); electrodes (12) are formed on the first substrate; a second substrate (21) facing the first substrate with a discharge space there between; a sealing layer (partition 24)

located between the first substrate and the second substrate, wherein the sealing layer (partition wall) has a thermal expansion coefficient of approximately $65 \times 10^{-7} \sim 80 \times 10^{-7}/^{\circ}\text{C}$ (see Table 3, example 26); at least one of a buffer layer or a dielectric layer (13) formed between the first substrate and the sealing layer (paragraph 0057), wherein the at least one of the buffer layer or the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B2O3 at a ratio of 10% to 20% and SiO2 at a ratio of 15%-25%; (see Table 1B, example no. 15 paragraph 0260) and a protective film (14) formed on the at least one of the buffer layer or the dielectric layer.

Regarding claim 3, Tanaka et al. disclose that the buffer layer has a thermal expansion coefficient different from a thermal expansion coefficient of the first substrate (see Table 2 & Table 3).

Regarding claim 5, Tanaka et al. disclose that the buffer layer has a thermal expansion coefficient different from a thermal coefficient of the sealing later (partition layer is made of alumina different from the composition of buffer layer (paragraph 0237: see Table 3).

Regarding claim 7, Tanaka et al. disclose that the first substrate has a thermal expansion coefficient of approximately $80 \times 10^{-7} \sim 95 \times 10^{-7}/^{\circ}\text{C}$ (Table 2 of page 13).

Regarding claim 9, Tanaka teaches all the limitation of claim 9, including the composition of the buffer or dielectric layer (see rejection of claim 1) but is silent about the thermal expansion coefficient (CTE) of that composition (see in table 1B, example 15, thermal expansion coefficient is not mentioned). However, CTE is the intrinsic property of a material or composition. Since Tanaka et al. disclose the same composition of the dielectric or buffer layer

as claimed, it has intrinsically the same CTE range as claimed since material and its properties are inseparable.

Regarding claims 26 & 41, Tanaka et al. disclose a plasma display panel (see Figs 1 & 2), comprising: a first substrate (101); electrodes (102) are formed on the first substrate; a second substrate (105) arranged with respect to the first substrate such that a discharge space is provided there between; a sealing layer (108 & 24) between the first substrate and the second substrate, the sealing layer (partition wall) a thermal expansion coefficient of approximately $65 \times 10^{-7} \sim 80 \times 10^{-7}/^{\circ}\text{C}$ (see Table 3, example 26); and at least one of a buffer layer or a dielectric layer (103) formed between the first substrate and the sealing layer, wherein the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient of approximately $72 \times 10^{-7}/^{\circ}\text{C}$ to thermal expansion coefficient (paragraphs 9-11 & 21).

Regarding claim 27, Tanaka et al. disclose the plasma display, wherein the sealing layer extends in a longitudinal direction from a first end (upper end) to a second end (lower end), the first end located proximal to the first substrate and the second end located proximal to the second substrate, the buffer layer provided only in the area between the first end of the sealing layer and the first substrate (see Fig 1).

Regarding claim 28, Tanaka et al. disclose another sealing layer (partition wall at the other end of device opposite to the one end, Fig 1) between the first substrate and the second substrate; and another buffer layer (end part of the buffer layer between another end partition wall 24 and the substrate) provided between the first substrate and the another sealing layer,

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being intermediate between first substrate and another sealing layer another buffer layer will compensate thermal stress between first substrate and the sealing layer.

Regarding claim 30, Tanaka et al. disclose that the thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the first substrate (first substrate is made of soda lime glass which has thermal expansion coefficient which is different from buffer layer 103, see paragraph 0021 and table 2 of page 13).

Regarding claim 31, Tanaka et al. disclose that the thermal expansion coefficient of the buffer layer (103) is different from the thermal expansion coefficient of the sealing layer (partition wall; see paragraph 0023).

Regarding claim 39, Tanaka et al. disclose that the dielectric layer has the following composition: PbO at a ratio of 45% to 55%, B2O3 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25% (see Table 1B, example no. 15 paragraph 0260).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 32, 36 & 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Ebihara et al. (US 6514111).

Regarding claims 32 and 42, Ebihara discloses in Fig1, a plasma display comprising: a first substrate (2); a second substrate (7) arranged with respect to the first substrate (2) such that a discharge space is provided there between; a sealing layer (12) between the first substrate (2) and the second substrate (7); at least one of a buffer layer (4) or a dielectric layer provided on the first substrate (2) and provided between the first substrate (2) and the sealing layer (12); wherein the buffer layer (4a) has a thickness of 35 Micron between the sealing layer and the first substrate (lines 19-22 of column 6) and a protective layer (6) on the dielectric layer and further comprising plurality of electrodes (3) on the first substrate .

However, Ebihara fail to explicitly disclose that the thickness is greater than the 35 Micron. However, Ebihara in Fig 4 illustrates dielectric layer thickness with crack occurring rate for particular aspect ratio and diagonal size of PDP, however, teaches that the range of thickness value can change depending on the size and aspect ration of the PDP (lines 19-22 of column 6).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to have thickness of the dielectric layer being greater than 35 micron in the device of Ebihara for different aspect ratio and size of PDP, since such thickness is dependent on the size of the PDP.

Regarding to claim 36, Ebihara discloses that the at least one of the buffer layer (24) or the dielectric layer is the buffer layer (24a), and the dielectric layer (25) is formed on the buffer layer (24) such that the buffer layer (24) is provided between the first substrate (22) and the dielectric layer (25) and such that the dielectric layer (25) is provided between the buffer layer (24) and the protective film (26, see Fig 2B).

Claims 11-13, 29 & 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., as applied to claims 1 & 26 above, and further in view of Ebihara et al. (US 6514111).

Regarding claim 11-13, Tanaka et al. disclose all the limitations of claims 11-13 except for buffer layer together with a dielectric layer such that the buffer layer is provided between the first substrate and the dielectric layer and such that the dielectric layer is provided between the buffer layer and the protective layer wherein the buffer layer is formed to be extended from the dielectric layer and buffer layer is formed of a different material from that of dielectric layer. However, Ebihara, in the same filed of Plasma display panel, discloses in Figures 2A-C, the dielectric layer (25) and the buffer layer (24) such that the buffer layer (24a) is provided between the first substrate (22) and the dielectric layer (25) and such that the dielectric layer (25) is provided between the buffer layer (24a) and the protective film (26) and the buffer layer (24) extends from the dielectric (see region 24a) and buffer layer 24 is formed from a different material than the dielectric layer 25 (see materials having different softening points; lines 41-65 of column 6), such arrangement of dielectric layer having greater thickness in the discharge region while lower thickness in the sealing area, reduces the stress in the dielectric layer of the sealing region thereby occurrences of flaws is avoided with out reducing the thickness of the dielectric layer in the discharge region which is needed for ac plasma (lines 39-44 of Col.3). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a dielectric layer on the buffer layer as taught by Ebihara et al. in the device of Tanaka, since this will reduce the stress in the dielectric layer of the sealing region thereby

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occurrence of flaws is avoided without reducing the thickness of the dielectric layer in the discharge region which is needed for ac plasma.

Regarding claim 29, Tanaka et al. discloses all the limitations of claim 29 except for another upper dielectric layer formed on the substrate between the buffer layer and the another buffer layer.

However, Ebihara et al. discloses a plasma display panel comprising an upper dielectric layer (25) formed on the first substrate between the buffer layer (24a) and the another buffer layer (opposite side 24a); and a protective film formed on the upper dielectric layer (25, see Fig 2C) for the purpose of increasing the thickness of the dielectric layer in the discharge region which is needed for AC plasma display to avoid dielectric breakdown, while having thinner dielectric layer in the sealing region.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add another upper dielectric layer (25) as taught by Ebihara to increase the thickness of the dielectric layer in the discharge region to avoid dielectric breakdown during AC plasma discharge.

Regarding claims 44-45, Tanaka fails to disclose that the buffer layer (4a) has a thickness greater than 35 Micron and less than 39 micron between the sealing layer and the first substrate (lines 19-22 of column 6).

However, Ebihara discloses thickness of the dielectric layer being 35 micron. Further, in Fig 4, Ebihara teaches the experimental results of variation of thickness of dielectric layer with crack occurring rate for particular aspect ratio and diagonal size of PDP, however, teaches that

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the range of thickness value can change depending on the size and aspect ratio of the PDP (lines 19-22 of column 6).

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to have thickness of the dielectric layer being greater than 35 micron in the device of Ebihara for different aspect ratio and size of PDP, since such thickness is dependent on the size of the PDP.

Claims 34-35 & 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebihara et al. as applied to claim 32 above, and further in view of Tanaka et al. (US 2002/0036466).

Regarding claims 34-35 & 43, Ebihara et al. disclose all the limitations of claims 34-35, & 43 except for composition of the buffer or dielectric layer being PbO at a ratio of 45% to 55%, B2O3 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25%. and CTE of the composition is greater or equal to $72 \times 10^{-7}/^{\circ}\text{C}$, while the sealing layer (partition layer 24) has a thermal expansion coefficient approximately $65 \times 10^{-7} \sim 80 \times 10^{-7}/^{\circ}\text{C}$ (see Table 3, example 26) .

However, Tanaka et al. in the same field of plasma display panel teaches a dielectric layer having the same composition (see table 1B, example 15, paragraph 0260), though not mentioned, since composition of the dielectric layer is same as claimed composition it would intrinsically have same CTE, since CTE is the intrinsic property of a material/composition.

Further Tanaka teaches that use of such dielectric materials in the plasma display produce less cracks in the dielectric layer (see paragraph 0030).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the dielectric material as disclosed by Tanaka et al. in the device of Ebihara, since such dielectric layer would provide less cracks.

Response to Arguments

Applicant's arguments filed on 3/6/2008 have been fully considered but they are not persuasive.

Applicant contends that the limitation of previous claim 8, which has been now incorporated in claim 1 is not taught by Tanaka. Further Tanaka's table 3, Example 26 corresponds to thermal expansion coefficient of dielectric layer, not sealing layer.

Examiner respectfully presents that Tanaka's Table 3 example 26, teaches the thermal expansion layer of alumina, and column 6 of table 3 shows the composition of partition or sealing layer which is also made of alumina, thus sealing layer has the claimed thermal expansion coefficient.

Regarding applicant's argument against claim 32 (page 13 of Remark), examiner respectfully differs, since Ebihara explicitly disclose that the range 35 is not rigid, however, it can vary depending on the aspect ratio and size of the PDP.

Further it is noted that applicant in the specification discloses thickness range being 5-50 micron, and does not disclose any critically for the specific range of thickness greater than 35 micron to less than 39 micron which does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of optimization, which a person of ordinary skill in the art would have found

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obvious to experiment suitable thickness of the dielectric layer for particular PDP in order to prevent cracking of the dielectric layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is 571-272-2452. The examiner can normally be reached on Monday-Friday 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minh-Toan Ton can be reached on 571-272-2303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Karabi Guharay/
Primary Examiner, Art Unit 2889